International Journal of Electrical, Electronics and Computer Engineering **4**(2): 34-41(2015)

ISSN No. (Online): 2277-2626

Register Cell Design using High Speed Low Power D Flip-Flop with Domino Feed through Logic

Padma Khare* *and Shaista Anjum*****

**Research Scholar, Department of Electronic and Communication Engineering, LNCT, Bhopal, (MP), INDIA*

***Assistant Professor, Department of Electronic and Communication Engineering, LNCT, Bhopal, (MP), INDIA*

(Corresponding author: Padma Khare)

(Received 03 June, 2015 Accepted 12 August, 2015)

(Published by Research Trend, Website: www.researchtrend.net)

ABSTRACT-- in this paper a low-power high-speed CMOS Domino logic family called as Domino feed through logic is used for high speed and low power operation using this technique a low-power high-speed FTL logic for register is presented. The proposed registers uses feed through Domino logic to implement on 90 nm CMOS technology and simulated using micro-wind simulation tool. The concept is very fined through intensive simulation at different temperature levels and different capacitive load. Here we implemented 4 bit register cell using D flip-flop and the D flip-flop is implemented using NAND gate, and each NAND gate is implemented using Domino feed through logic. The dynamic power reduction is 80% for LP-FTL and 58% for HS-FTL with respect to normal CMOS domino logic.

I. INTRODUCTION

Reduction of power in compromise with performance of the circuit is the great interest of area for analog and digital electronics engineer. There are various designing techniques for digital circuits are proposed in the last two decades which optimizes static and dynamic losses of the electronic circuits either using dual threshold transistor or dual voltage supply[3]. There are many different logic circuit design techniques as CMOS, Bi CMOS, NMOS, Pseudo NMOS, differential cascade voltage swing logic(CVSL), pass transistor logic, dynamic CMOS logic, Domino logic e.t.c [2,4]. In all of above Domino logic generally used for high performance integrated circuits the advantages are rail-to-rail logic swing, the small silicon area, a small parasitic capacitance, glitches free operation and the logic will design with a small number of transistor counts as compared CMOS logic design. This advantage of Domino logic circuits are noise in circuit due to leakage current and charge sharing & charge distribution problem [5,6,7]. Only noninverting structures are possible due to presence of inverting buffer and large power consumption as compared to CMOS logic design. To decrease the power consumption of Domino CMOS logic a new logic family named as feed through logic (FTL) is proposed.

In this technique the output is evaluated before all the inputs are valid (active) using Domino logic. This feed through increases the performance of Domino logic, either it will be combinational or sequential, are the disadvantages of Domino logic are completely diminished using this logic [8].

The dynamic logic uses high voltage supply for logic evaluation and low supply voltage for clocking dynamic circuit. This will increases static power loss in dynamic circuit.

The dynamic power consumption in CMOS circuits is given by

$$P_{dynamic} = V_{dd} F_{clk} \sum_{i} V_{i,swing} C_{i,load} \alpha_i$$

Where $V_{i,swing}$ is the voltage swing at the load, $C_{i,load}$ is the capacitive load at the node, α_i is the switching factor, F_{clk} system clock frequency, V_{dd} supply voltage.

In this paper low-power and high-speed FTL circuit for four bit register is presented using D- flip-flop.

II. CONVENTIONAL DESIGN OF FTL

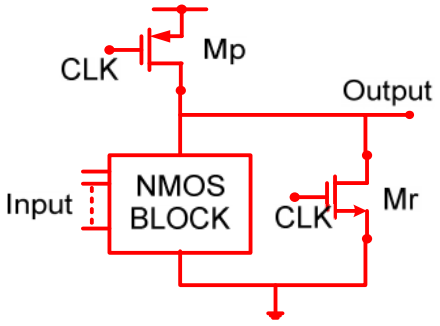

Fig. 1. Conventional design of FTL circuit.

The basic architecture of FTL is shown in the above figure.1 where NMOS Mr is used for the reset the output to low level work as pull-down and a PMOS Mp for pull-up the output node to high potential Vdd. The two Mp & Mr transistors is controlled by clock signal. As clk = 1(reset phase) Mr turn ON and the output is connected and the inverter is used to eliminate the circuit with other consultative circuit, when clk=0(evaluation phase) Mr is turned OFF and the output node conditionally arrange as output according to input NMOS block[8].

III. LOW POWER MODIFIED FTL (LP-FTL)

The modified low power FTL circuit is shown in Figure 2. This circuit reduces VOL (output low voltage) by using an additional PMOS pull up transistor MP2 in series with MP1. The circuit operation is similar to that of FTL [7]. During reset phase i.e. when CLK = high, output node is pulled to ground (GND) through Mr as in FTL operation. But during evaluation phase output node charges through Mp1 and Mp2. When CLK goes low (evaluation phase) Mr is turned off and the output node evaluates according to input block, to logic high (VOH) or low (VOL). The use of Mp2 is to reduce the VOL, as during evaluation phase when input evaluated the output to logic low, due to drain of Mp1 which is less than VDD, the output node goes low as compared to FTL circuit, this will reduce dynamic power consumption of circuit[1].

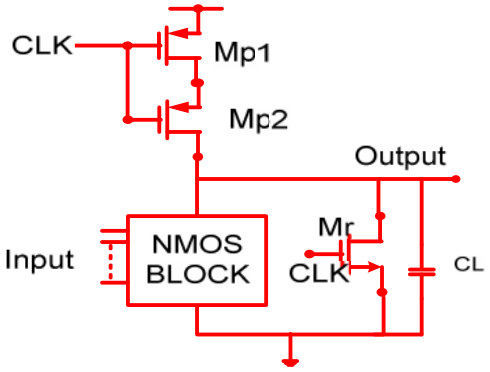

Fig. 2. NAND gate design using LP-FTL.

IV. HIGH SPEED PROPOSED MODIFIED FTL (HS-FTL)

To improve the speed of operation of LP-FTL circuit the reset transistor Mr is connected to VDD/2 as shown in Fig. The operation of this circuit is as follows, when CLK =high, the output node (OUT) will charges to the threshold voltage VTH of Mr transistor. During evaluation phase according to input block the output node only makes partial transition from VTH to VOH or VOL due to V^{th} it is easy to transit to VOH or VOL. Since during evaluation phase the output node (OUT) only makes partial transitions, this improves propagation delay. An inverter designed by using HS-FTL is shown in Fig. 3 [1].

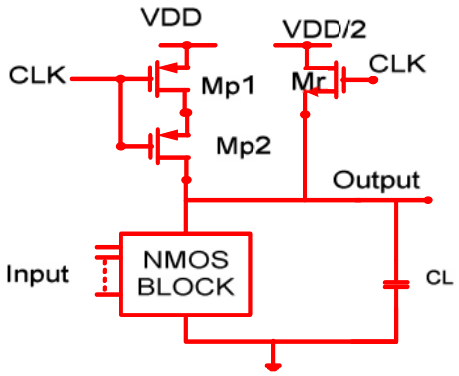

Fig. 3. NAND gate design using LP-FTL.

V. PROPOSED D REGISTER CELL DESIGN USING LP-FTL AND HS-FTL

A 4 bit register block diagram is shown in figure 4. And in the proposed D-register cell we use the LP-FTL and HS-FTL logic to design the D-Flip-flop the design of 4 bit D-flip-flop using NAND gate is shown in figure. 5 And the design of NAND gate is shown in figure 6 and figure 7 [11] using low power feed through logic and High speed feed through logic to design low power register cell and high speed register cell using domino logic .

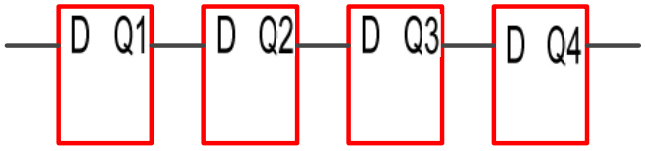

Fig.. 4. Bit register cell using D Flip-flop.

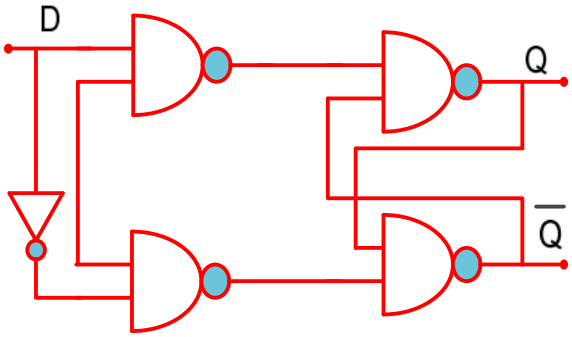

Fig. 5. D Flip-flop using NAND gate.

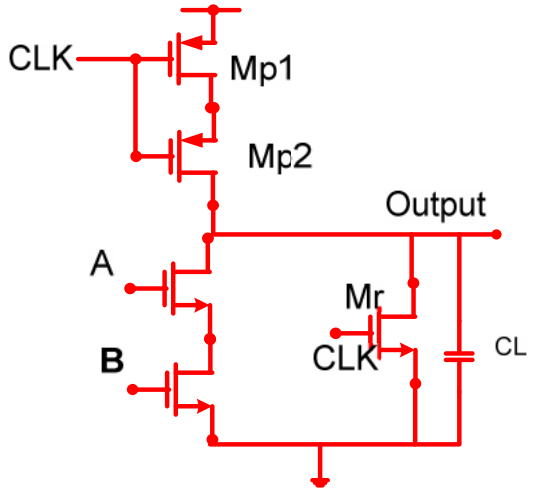

Fig. 6. NAND gate design using LP-FTL.

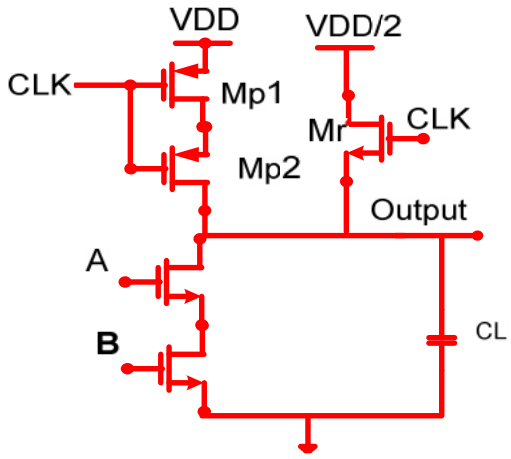

Fig. 7. NAND gate design using HS-FTL.

VI. PERFORMANCE ANALYSIS OF PROPOSED 4BIT REGISTER CELL USING LP-FTL AND HS-FTL

The two proposed modified 4 Bit register cell using Low power feed through logic and High speed feed through logic is designed on Microwind tool and simulated using CMOS 90nm technology at different temperature range from -20° to 120° at the supply voltage of 1V. Figure 8 shows layout diagram of high speed feed through logic (HS-FTL) of NAND gate and its simulation on Microwind 3.1 is shown in figure 9. Figure 10 shows layout diagram of low power feed (LP-FTL) through logic of NAND gate and its simulation on Microwind 3.1 is shown in figure 11.

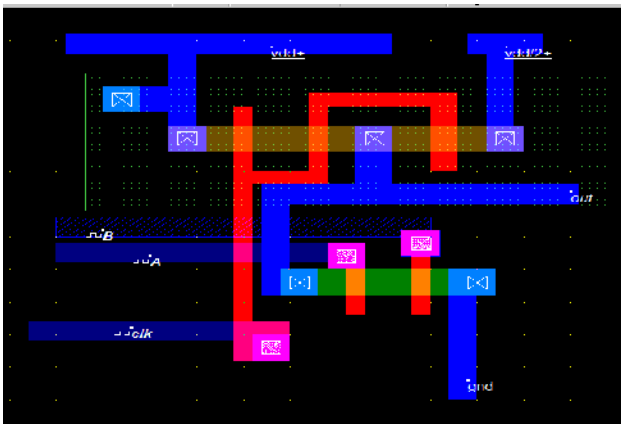

Fig. 8. Layout of HS-FTL of NAND gate.

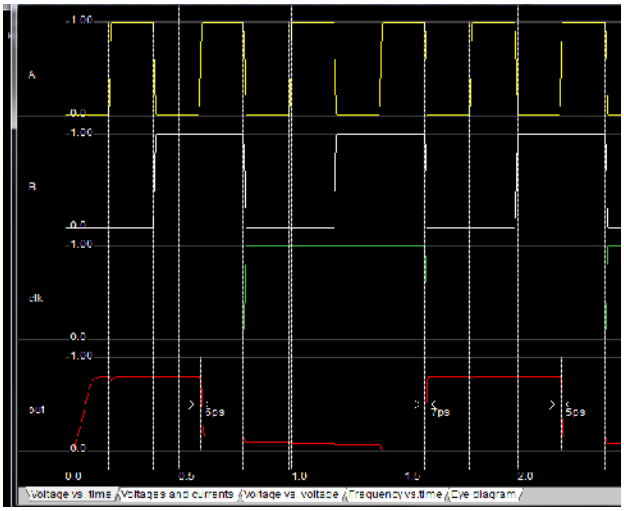

Fig. 9. Simulation of HS-FTL of NAND gate.

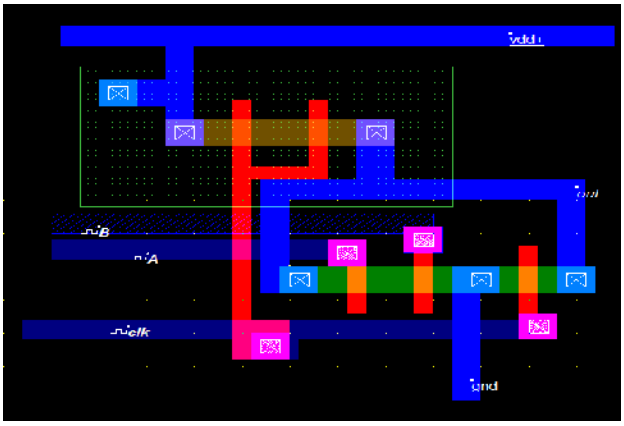

Fig. 10. Layout of LP-FTL of NAND gate.

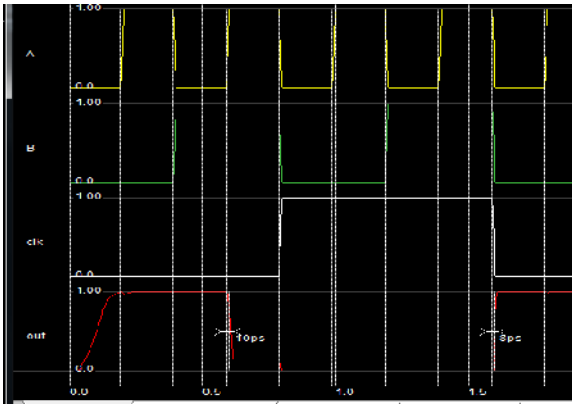

Fig. 11. Simulation of LP-FTL of NAND gate.

Figure 12 shows layout diagram of D flip-flop using CMOS NAND gate and its simulation on Microwind 3.1 is shown in figure 13.

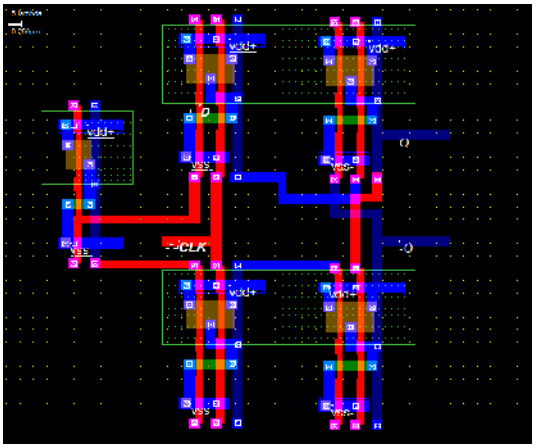

Fig. 12. Layout of Simple D Flip-Flop.

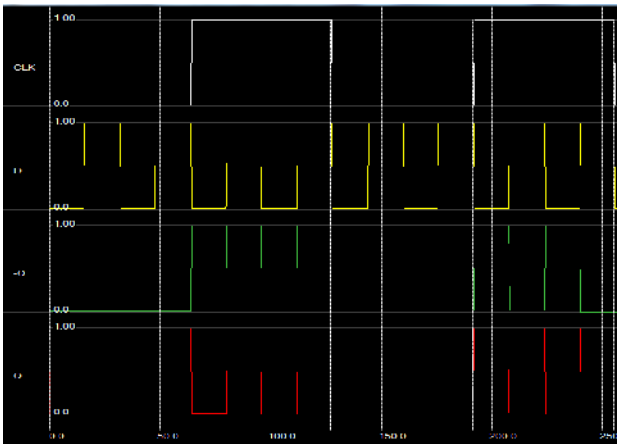

Fig. 13. Simulation of Simple D Flip-flop.

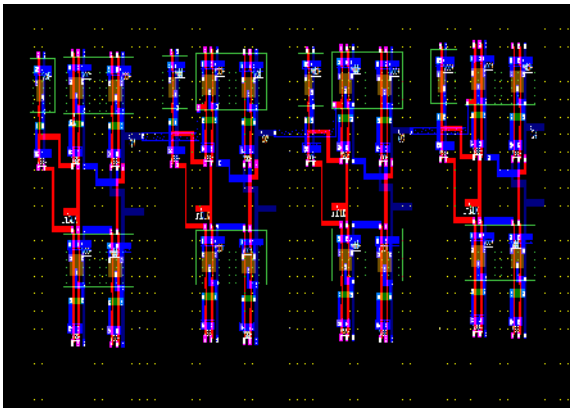

Fig. 14. Layout of 4 Bit D Register Cell.

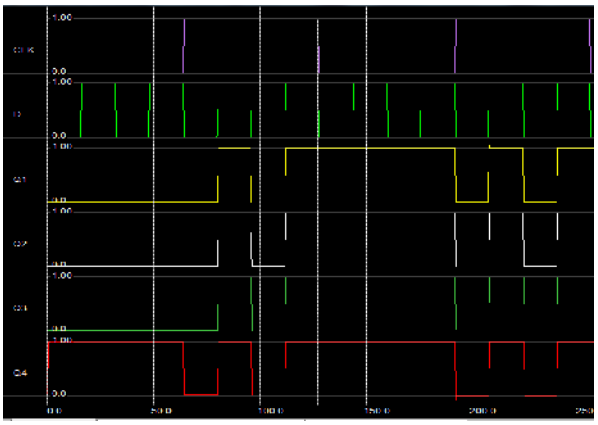

Fig. 15. Simulation 4 Bit D Register Cell.

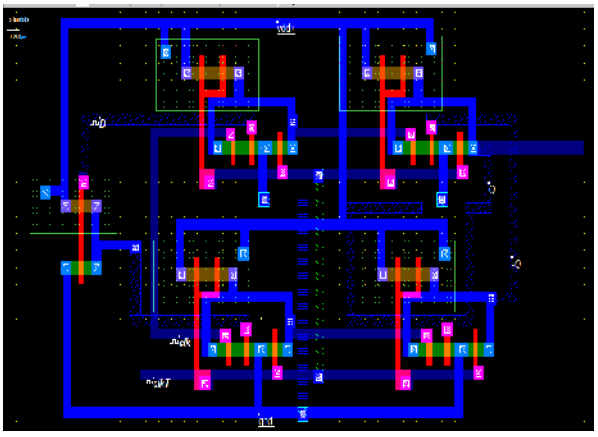

Fig. 16. Layout of LP-FTL D Flip-Flop.

Figure 14 shows layout diagram of 4 bit D register cell using CMOS NAND gate and its simulation on Microwind 3.1 is shown in figure 15. Figure 16 shows layout diagram of D flip-flop using low power feed through logic cell (LP-FTL) and its simulation on Microwind 3.1 is shown in figure 17.

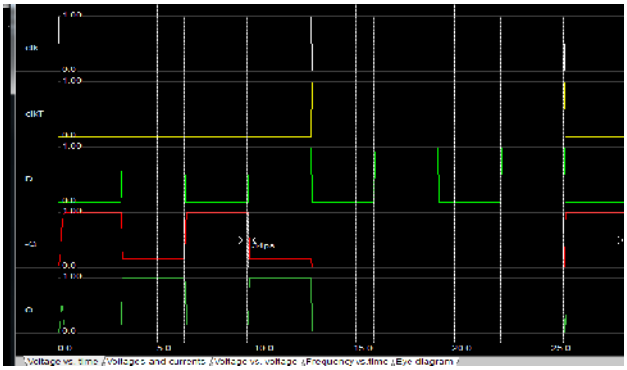

Fig. 17. Simulation of LP-FTL D Flip-Flop.

Figure 18 shows layout diagram of 4-bit D register cell using low power feed through logic cell (LP-FTL) and its simulation on Microwind 3.1 is shown in figure 19.

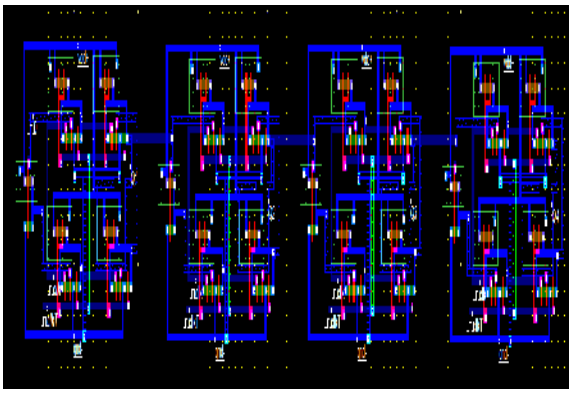

Fig. 18. Layout of LP-FTL 4 Bit D Register Cell

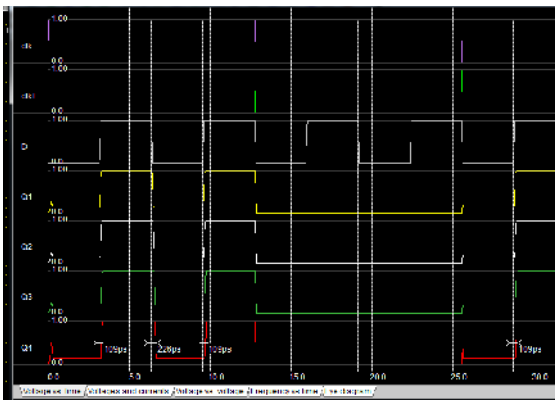

Fig. 19. Simulation of LP-FTL 4 Bit D Register Cell.

Figure 20 shows layout diagram of D flip-flop using high speed feed through logic cell (HS-FTL) and its simulation on Microwind 3.1 is shown in figure 21

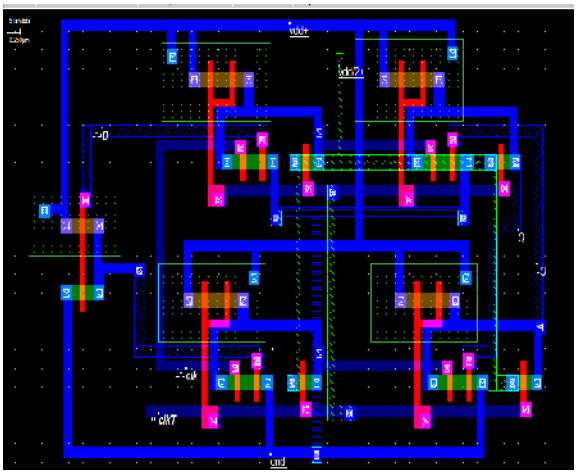

Fig. 20. Layout of HS-FTL D Flip-Flop.

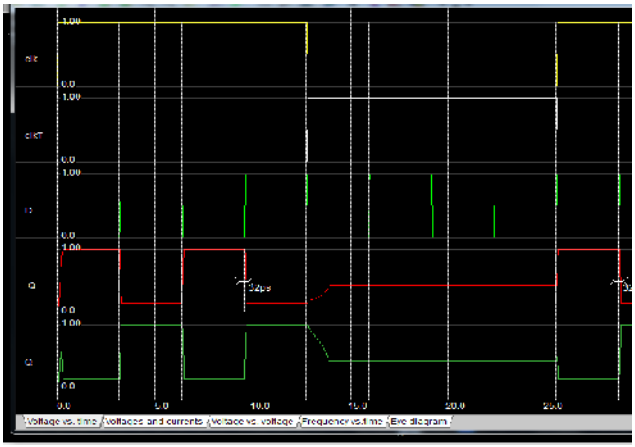

Fig. 21. Simulation of HS-FTL D Flip-Flop.

Figure 22 shows layout diagram of 4-bit D register cell using high speed feed through logic cell (HS-FTL) and its simulation on Microwind 3.1 is shown in figure 23.

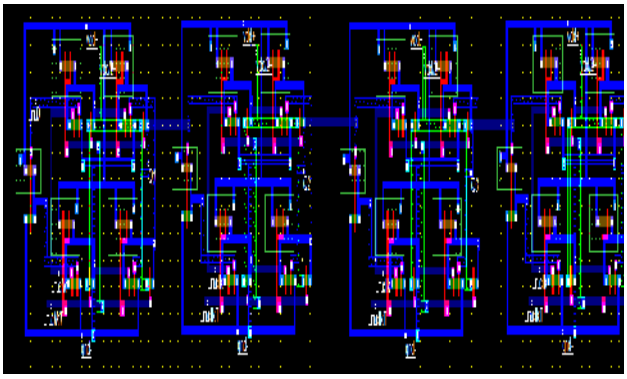

Fig. 22. Layout of HS-FTL 4 Bit D Register Cell.

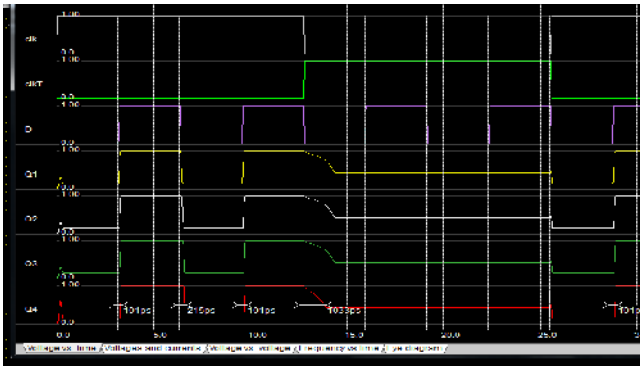

Fig. 23. Simulation of HS-FTL 4 Bit D Register Cell.

Table 1: Simulation result of simple 4 bit D register cell, LP-FTL 4 bit and HS-FTL 4bit register cell at 27° without load.

Logic family	Power (mW)	Delay(ps)	PDP(mW× ps)
Simple 4 bit register cell	1.4 mW	158ps	221.2
LP-FTL 4bit register cell	0.18mW	103ps	18.54
HS-FTL 4bit register cell	0.578mW	85ps	49.13

Figure 24 shows the propagation delay of simple D-flip flop using NAND gate , propagation delay low power feed through logic and high speed feed through logic with different temperature values range from -20° to 120°. Figure 25 shows the propagation delay of simple D-flip flop using NAND gate , propagation delay low power feed through logic and high speed feed through logic with different capacitive load values range from 1 to 20 fem to farad (fF).

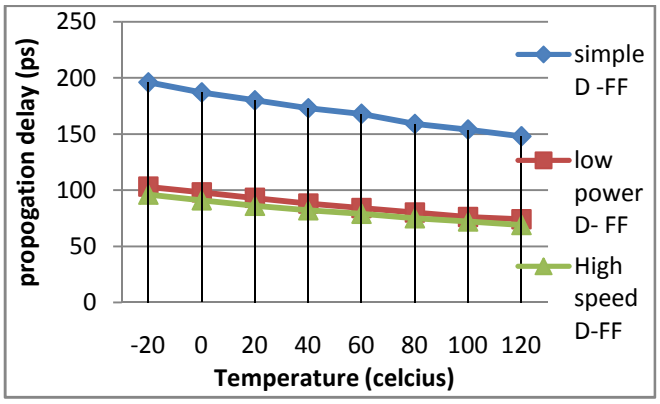

Fig. 24. Effect of temperature on propagation delay.

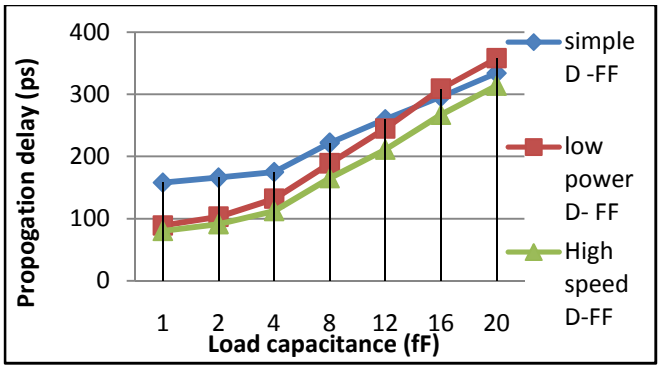

Fig. 25. Effect of capacitive load on propagation delay.

Figure 26 shows the power dissipation of simple D-flip flop using NAND gate, propagation delay low power feed through logic and high speed feed through logic with different capacitive load values range from 1 to 20 fem to farad (f F). Figure 25 shows the power delay product of simple D-flip flop using NAND gate, propagation delay low power feed through logic and high speed feed through logic with different capacitive load values range from 1 to 20 fem to farad (fF).

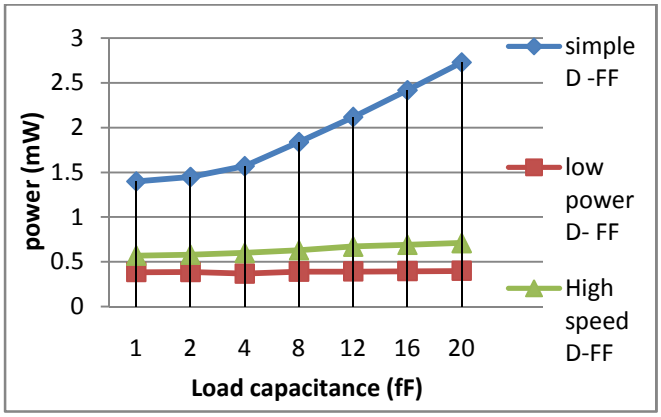

Fig. 26. .Effect of capacitive load on propagation delay.

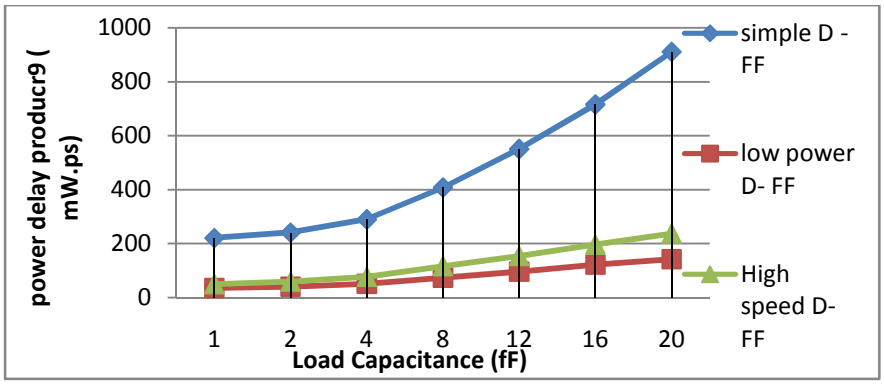

Fig. 27. Effect of capacitive load on power delay product.

CONCLUSION

In this paper Low power and high speed 4 bit D register cell is simulated on 90nm CMOS process technology from TSMC. The proposed LP-FTL D register and HS-FTL D register is compared with simple 4 bit D register normal cell the power consumption and delay of register cell is enhanced tangentially with due respect to normal 4 Bit CMOS flip flop.

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